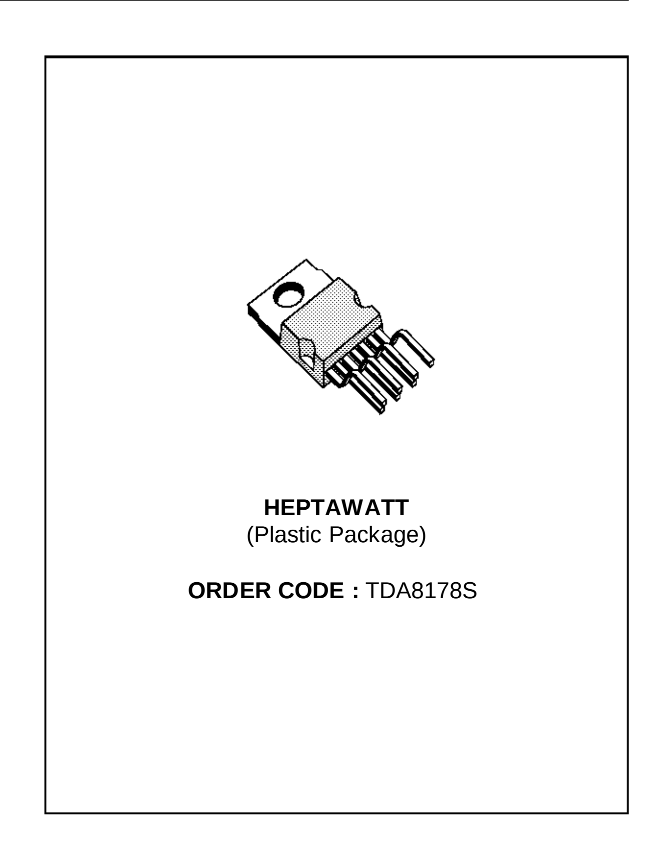


TDA8178S

TV VERTICAL DEFLECTION BOOSTER

- POWER AMPLIFIER
- FLYBACK GENERATOR
- THERMAL PROTECTION
- REFERENCE VOLTAGE



HEPTAWATT
(Plastic Package)

ORDER CODE : TDA8178S



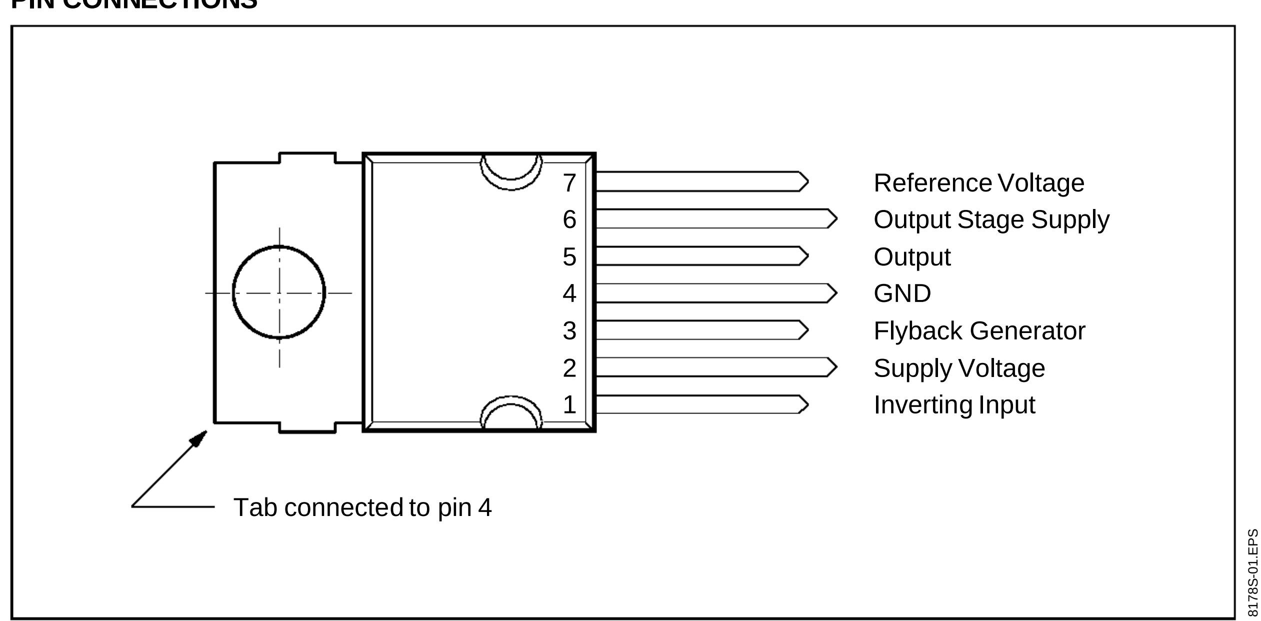
DESCRIPTION

Designed for monitors and high performance TVs, the TDA8178S vertical deflection booster delivers flyback voltages up to 90V.

The TDA8178S operates with supplies up to 42V and provides up to 2App output current to drive to yoke.

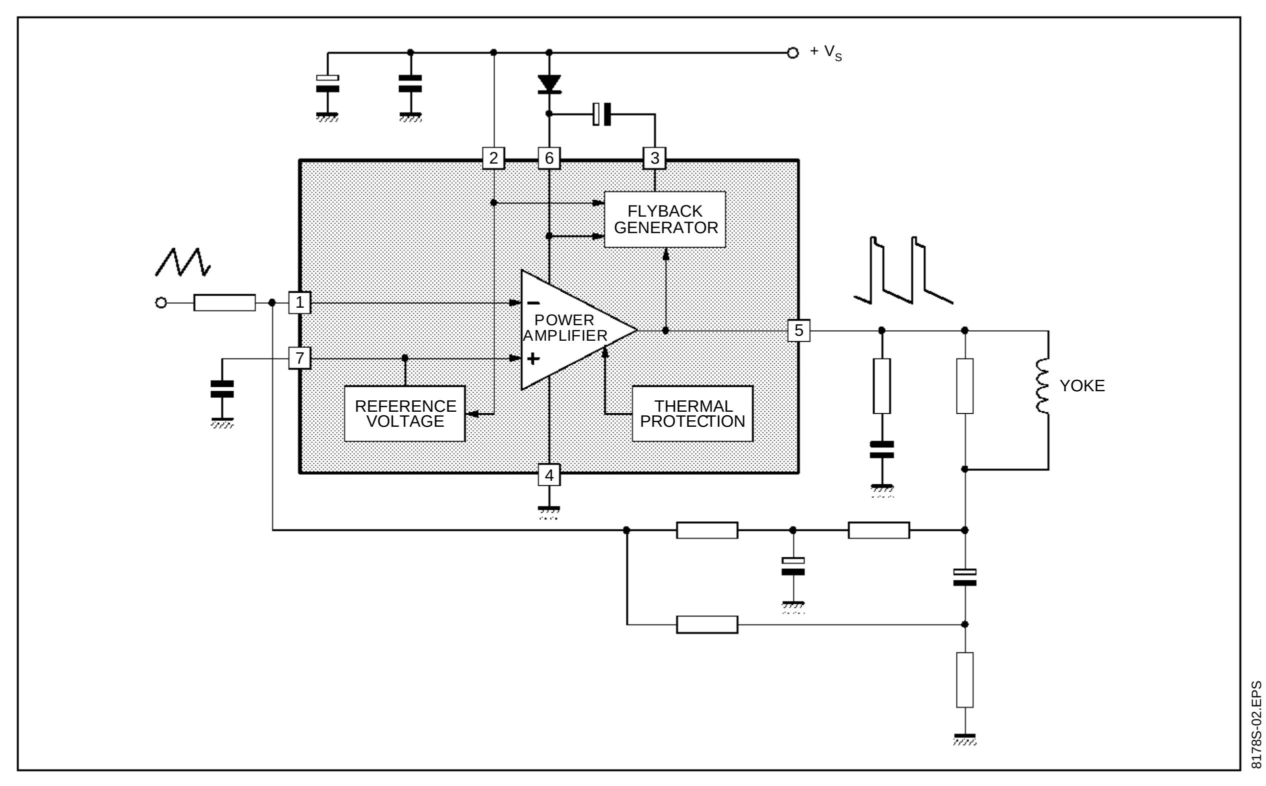
The TDA8178S is offered in HEPTAWATT package

PIN CONNECTIONS

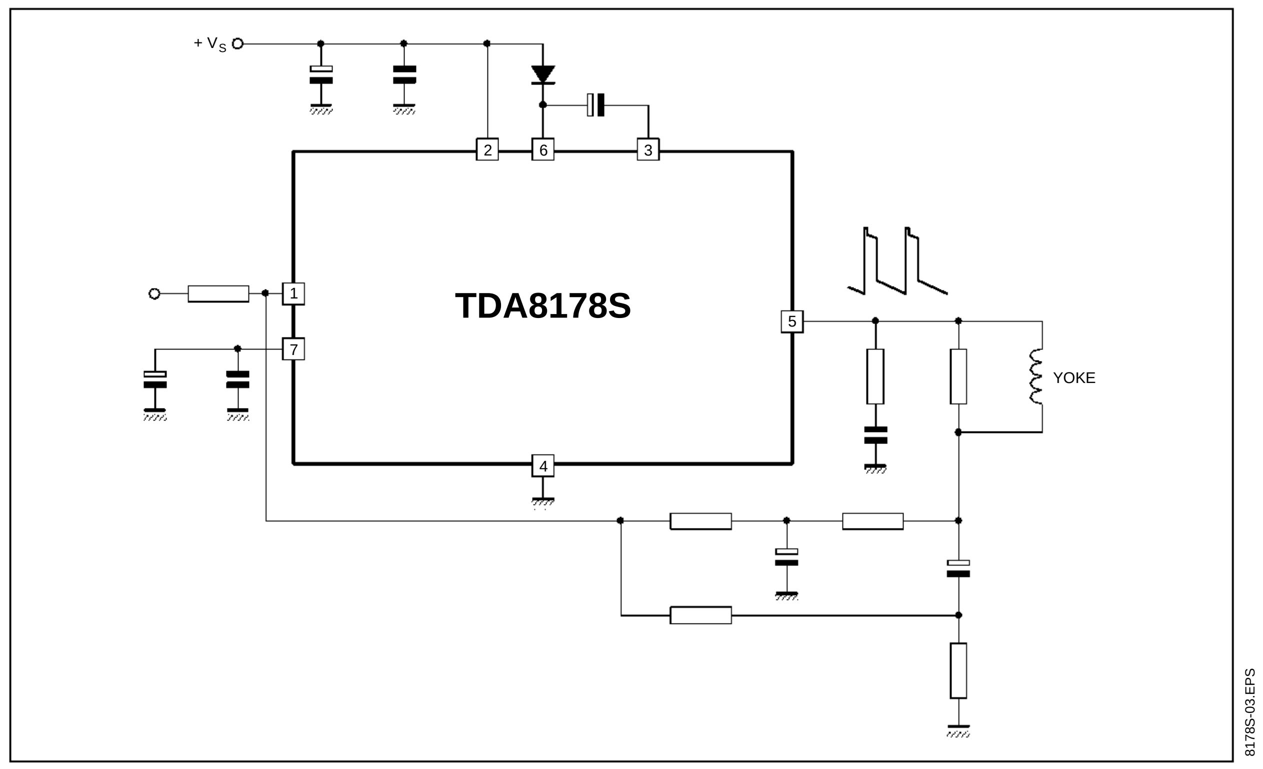


8178S-01.EPS

BLOCK DIAGRAM



APPLICATION CIRCUIT (V_S = 42V)



Note : For values see "Easy Design of Vertical Deflection Stages" (software available from our sales offices)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage (pin 2)	50	V
V_5 , V_6	Flyback Peak Voltage	100	V
V_1 , V_7	Amplifier Input Voltage	+ V_S	
I_O	Output Peak Current Non-repetitive, t = 2ms f = 50 or 60Hz, t ≤ 10µs f = 50 or 60Hz, t > 10µs	 2 2 1.8	A
I_3	Pin 3 DC at $V_5 < V_2$ Pin 3 Peak Flyback Current at f = 50 or 60Hz, $t_{fly} \leq$ 1.5ms	100 1.8	mA A
P_{tot}	Total Power Dissipation at T_C = 70°C	20	W
T_{stg}	Storage Temperature	- 40, + 150	°C
T_j	Junction Temperature	0, +150	°C

8178S-01.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j\text{-}c)}$	Junction-case Thermal Resistance	Max.	3	°C/W

8178S-02.TBL

ELECTRICAL CHARACTERISTICS

(V_S = 42V, T_A = 25°C, unless otherwise specified) (refer to the test circuits - see Figure 1 next page)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Operating Supply Voltage Range		10		42	V
I_2	Pin 2 Quiescent Current	I_3 = 0 I_5 = 0		10	20	mA
I_6	Pin 6 Quiescent Current	I_3 = 0 I_5 = 0		20	40	mA
I_1	Amplifier Bias Current	V_1 = 1V		- 0.2	- 1	µA
V_{3L}	Pin 3 Saturation to GND	I_3 = 20mA		1.3	1.8	V
V_5	Quiescent Output Voltage	V_S = 42V R_a = 3.9kΩ V_S = 35V R_a = 5.6kΩ	23.4 17	24.2 17.8	25 18.5	V
V_{5L}	Output Saturation Voltage to GND	I_5 = 1A		1.2	1.5	V
V_{5H}	Output Saturation Voltage to Supply	- I_5 = 1A		2.2	2.6	V
V_{D5-6}	Diode Forward Voltage between Pins 5-6	I_D = 1A		1.5	3	V
V_{D3-2}	Diode Forward Voltage between Pins 3-2	I_D = 1A		1.5	3	V
V_7	Internal Reference		2.1	2.2	2.3	V
$\Delta V_7/\Delta V_S$	Reference Voltage Drift versus V_S	V_S = 24 to 42V		2	4	mV/V
K_T	Reference Voltage Drift versus T_j	T_j = 0 to 125°C $K_T = \frac{\Delta V_7 \cdot 10^6}{\Delta T_j \cdot V_7}$		100	150	ppm/°C
R_1	Input Resistance			200		kΩ
T_j	Junction Temperature for Thermal Shutdown			140		°C

8178S-03.TBL

FIGURE 1 : DC Test Circuits

Figure 1a : Measurement of I_1, I_2, I_6, V_7, $\Delta V_7/\Delta V_S$

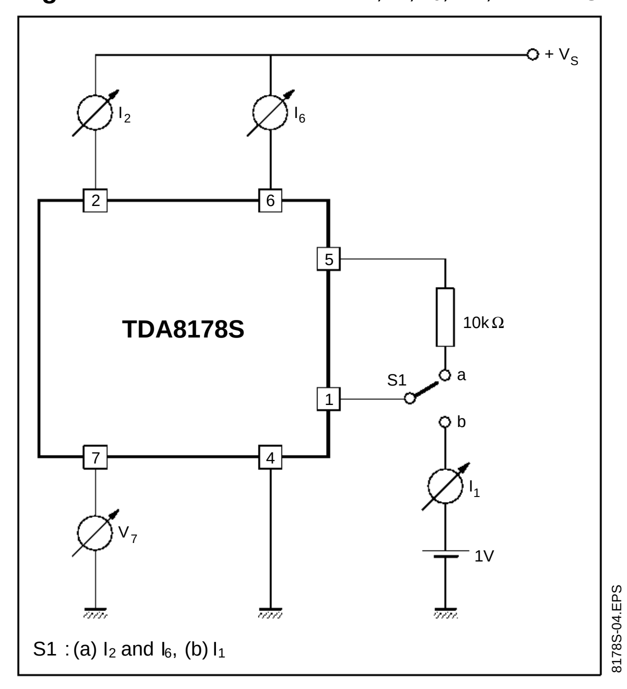


Figure 1b : Measurement of V_{5H}

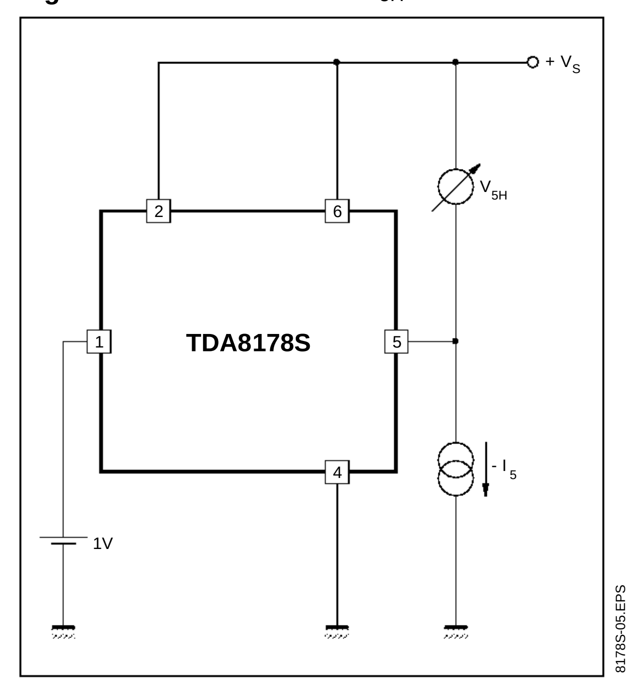


Figure 1c : Measurement of V_{3L}, V_{5L}

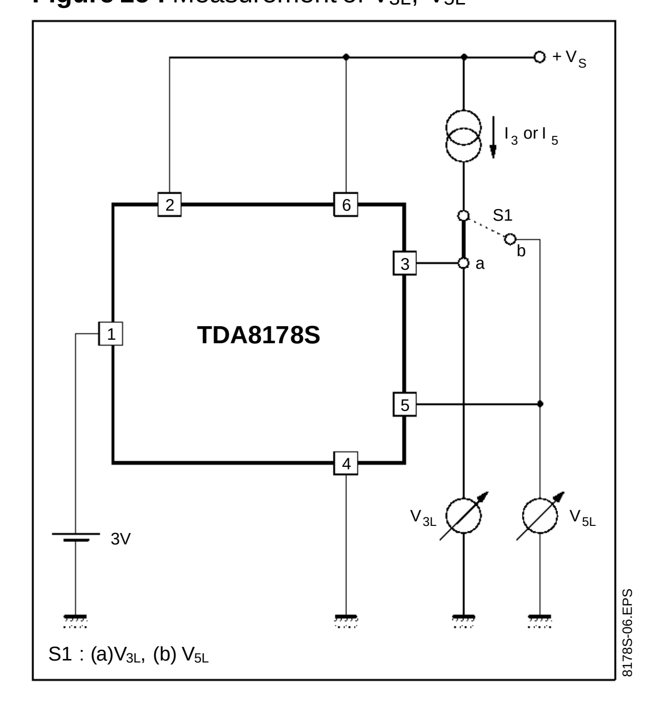


Figure 1d : Measurement of V_5

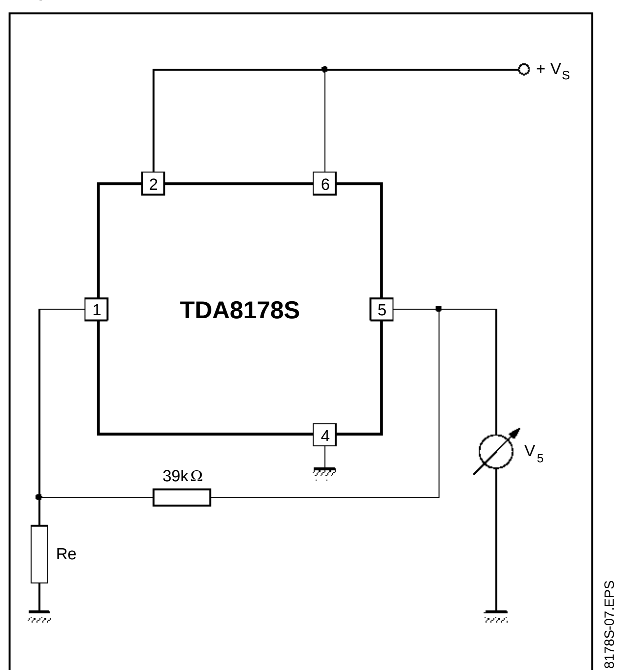
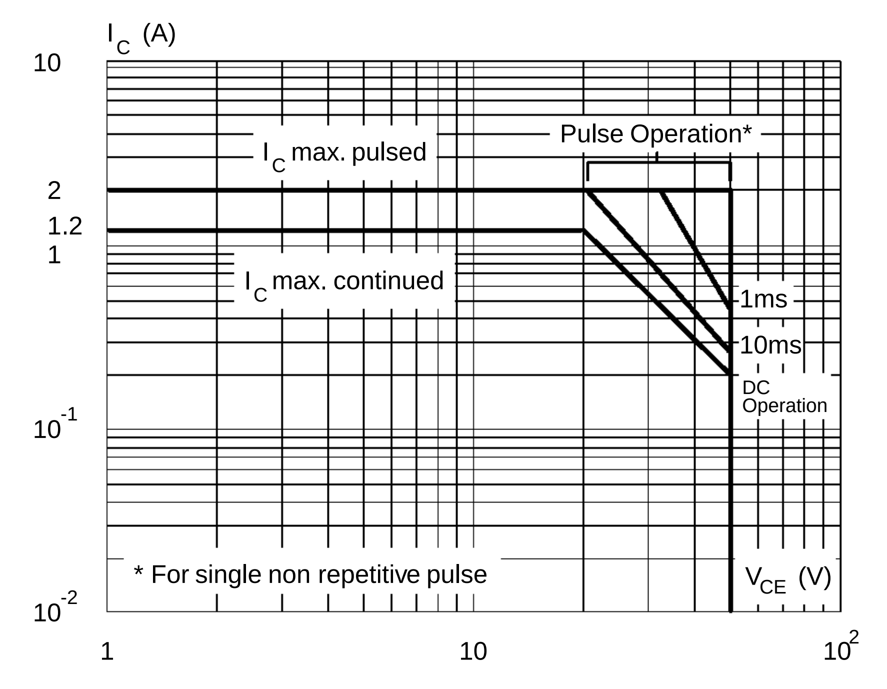
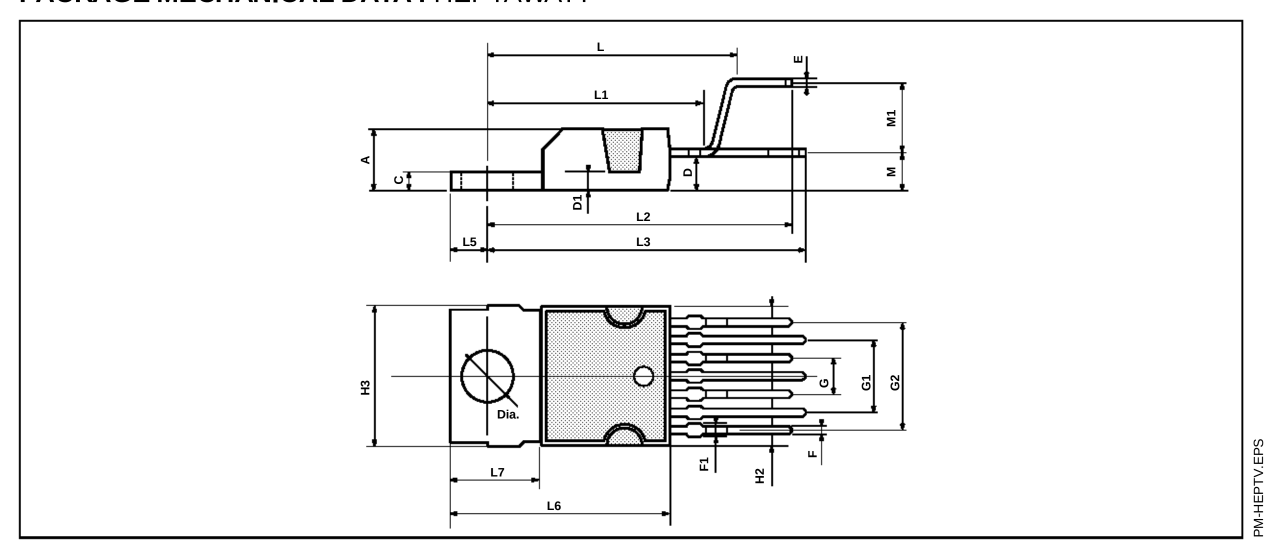


Figure 2 : SOA of Each Output Power Transistor at $T_A = 25^oC$



PACKAGE MECHANICAL DATA : HEPTAWATT



PM-HEPTV.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.6		08	0.024		0.031
F1			0.9			0.035
G	2.41	2.54	2.67	0.095	0.100	0.105
G1	4.91	5.08	5.21	0.193	0.200	0.205
G2	7.49	7.62	7.8	0.295	0.300	0.307
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L		16.97			0.668	
L1		14.92			0.587	
L2		21.54			0.848	
L3		22.62			0.891	
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
M		2.8			0.110	
M1		5.08			0.200	
Dia.	3.65		3.85	0.144		0.152

HEPTV.TBL

